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(54) Cooling semiconductor devices

(57) A semiconductor device comprises a semiconductor chip 21 including a substrate and a plurality of heat emissive elements formed on a surface portion thereof. The semiconductor chip 21 has a thermally conductive layer 23 formed on the chip so as to be in the proximity of the elements in order to conduct and dissipate heat produced by the elements. A thermally conductive plate 22 is provided adjacent the chip 21 and a heat discharging fin 24 is attached to the opposite side of the plate 22 from the chip 21. A second thermally conductive plate 26 and a cooling fin 27 are also provided. In a modification the device is mounted in a duct supplied with cooling fluid.

FIG.4

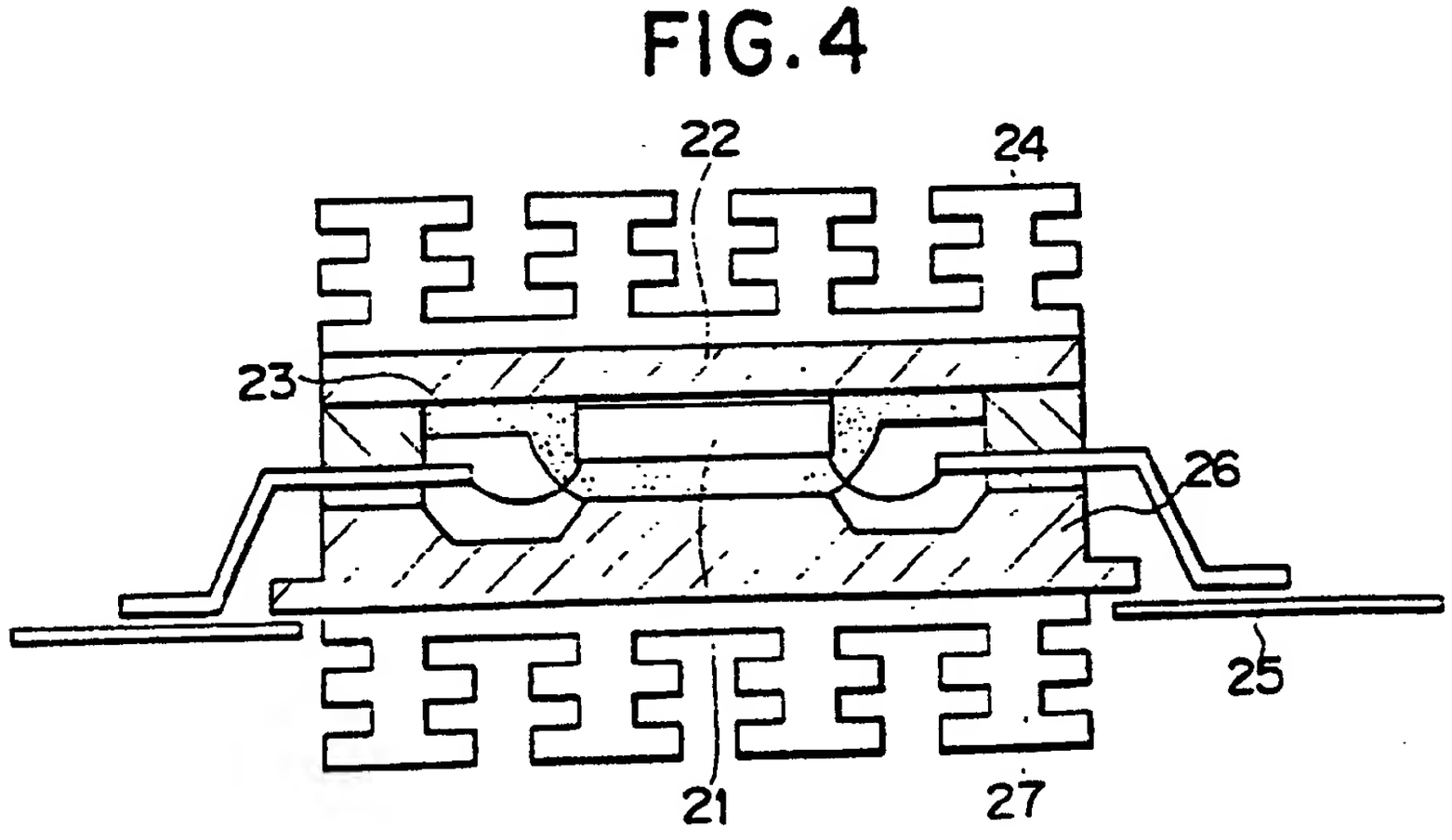

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FIG.1

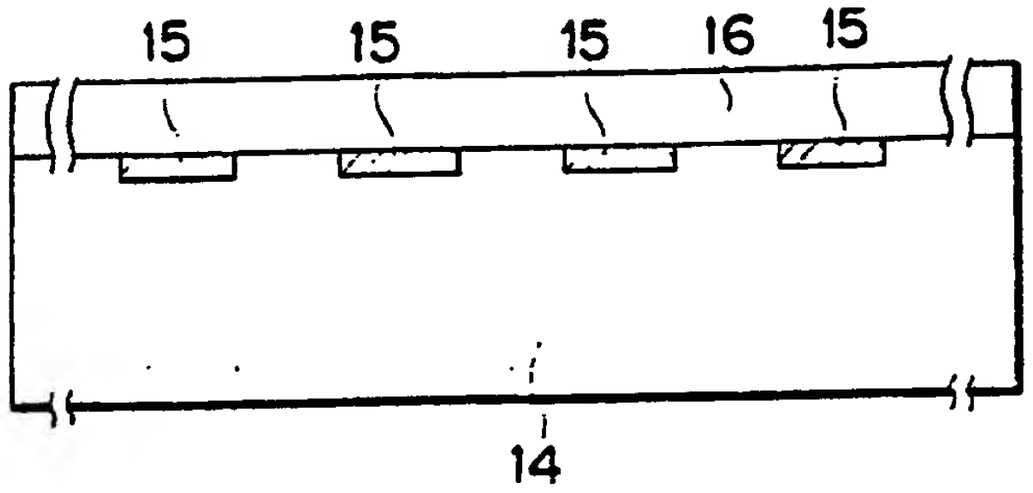


FIG.2

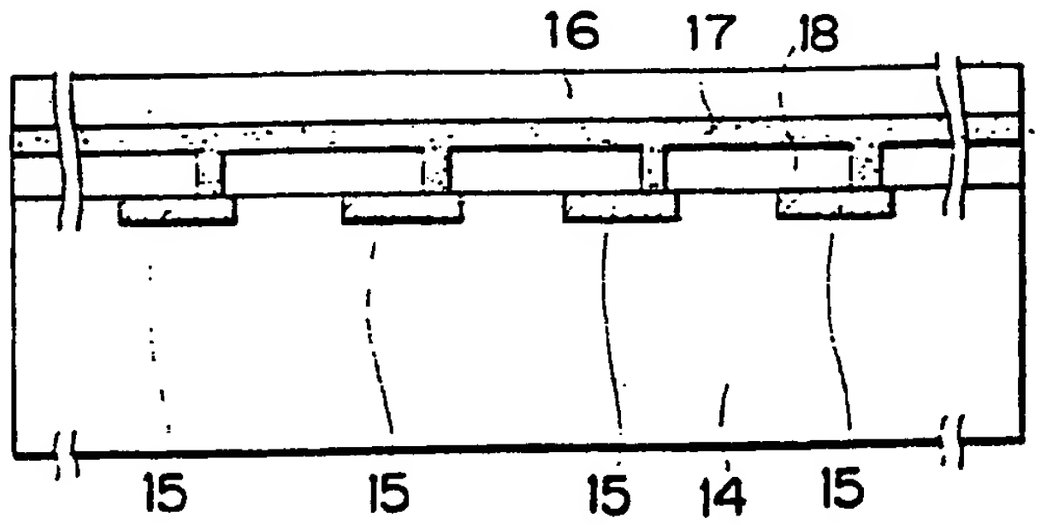


FIG. 3

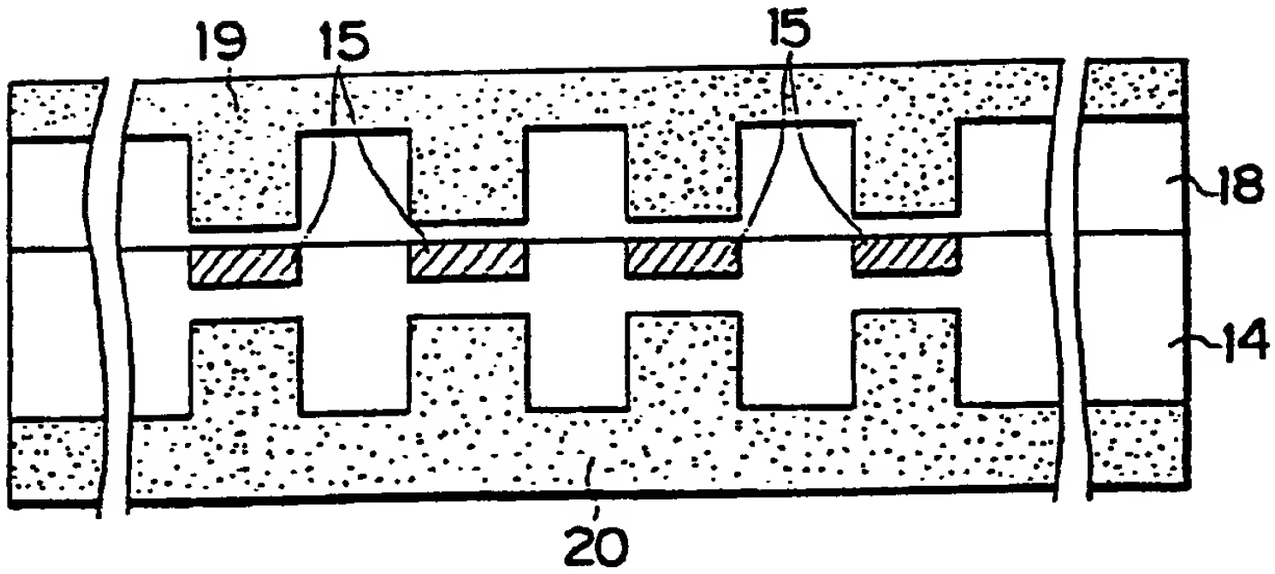


FIG. 4

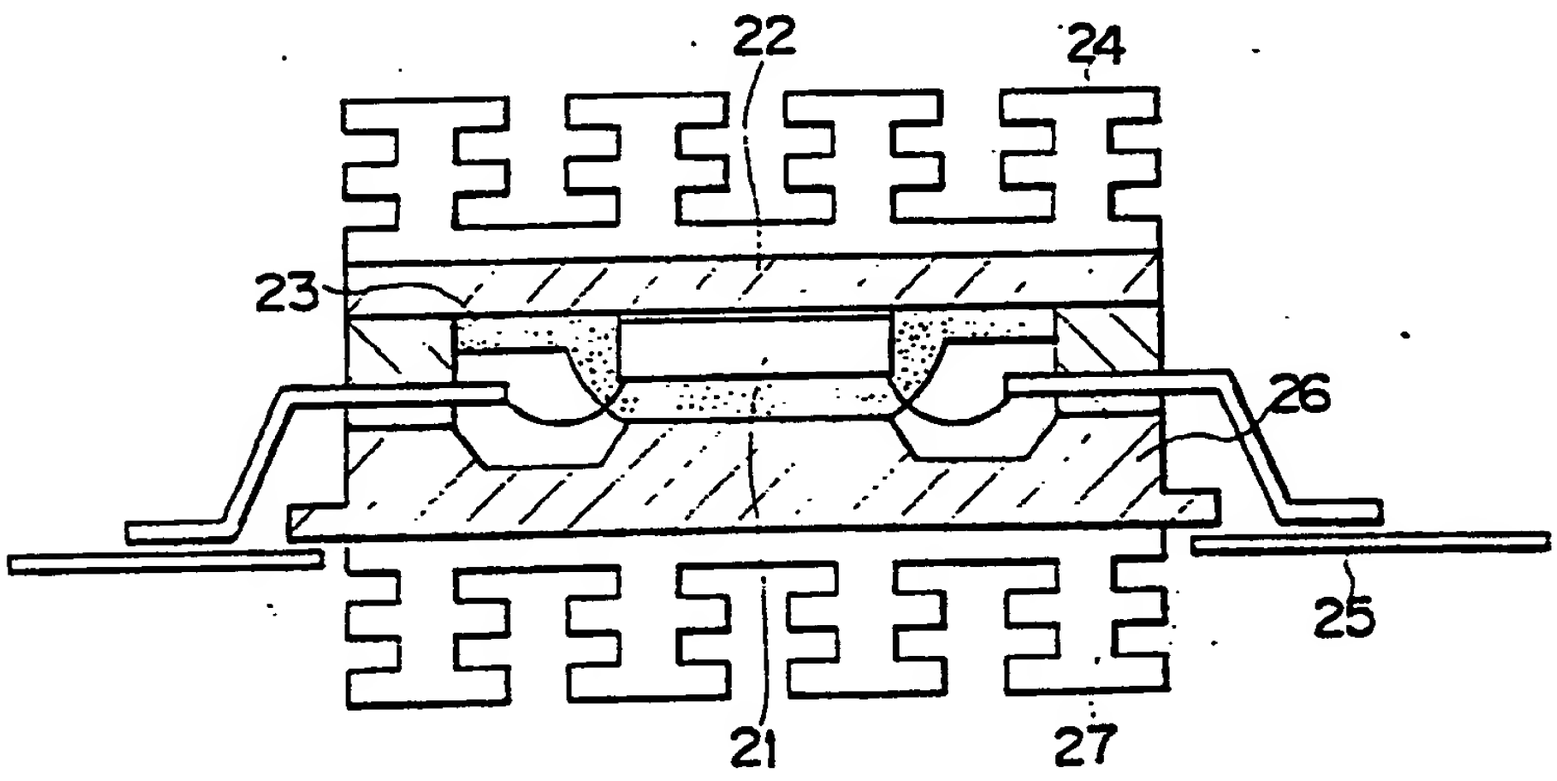


FIG. 5

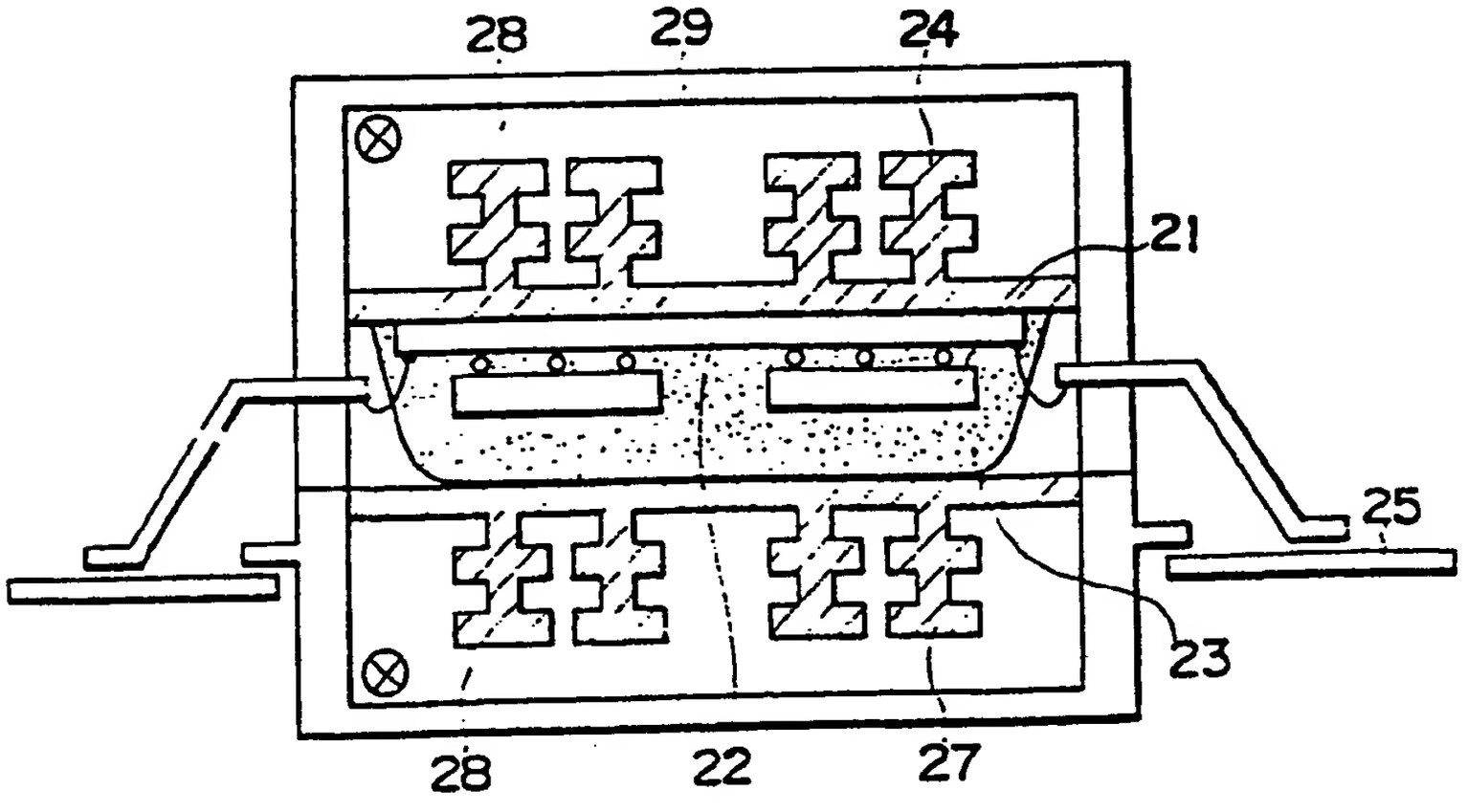


FIG. 6
PRIOR ART

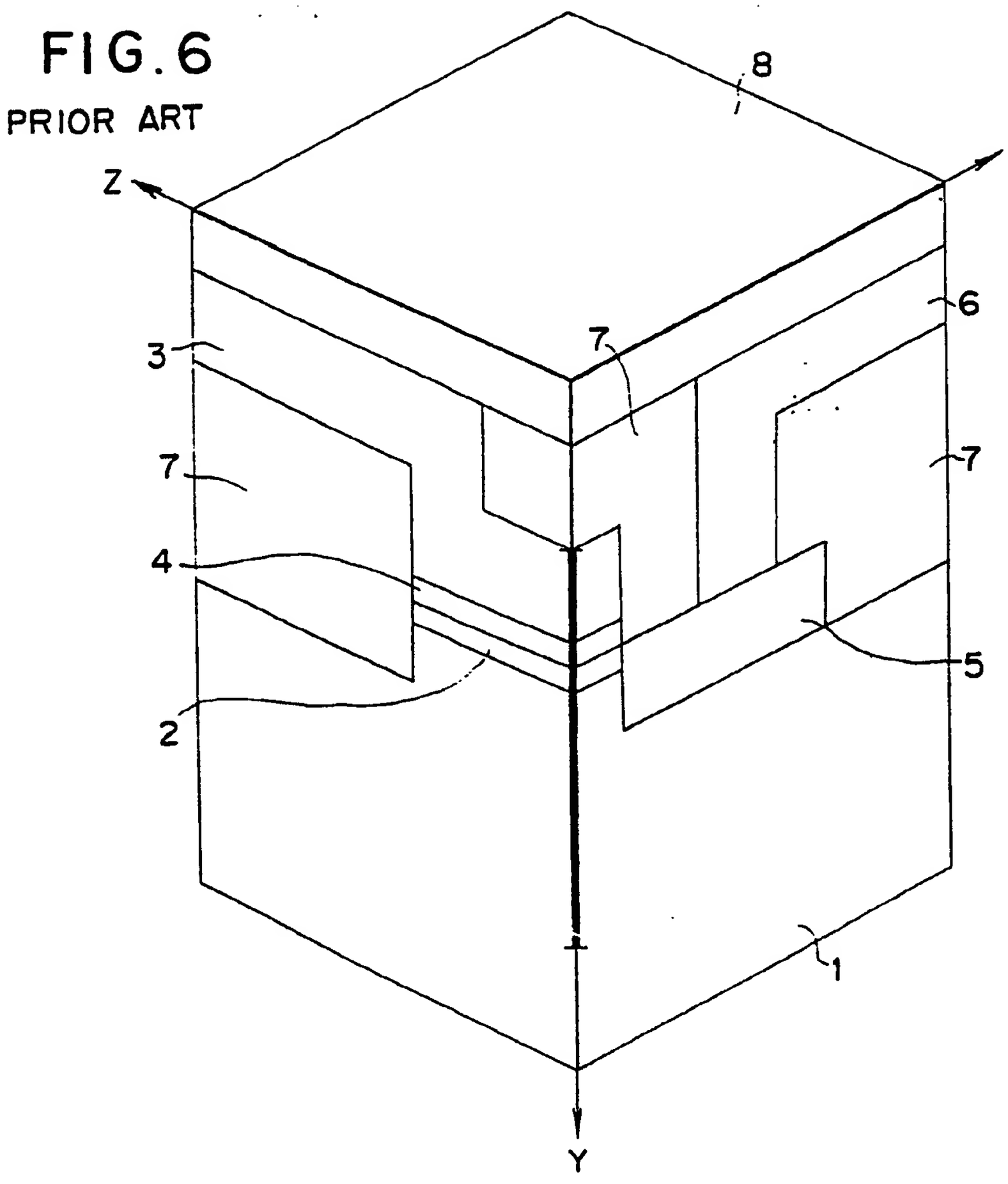


FIG.7

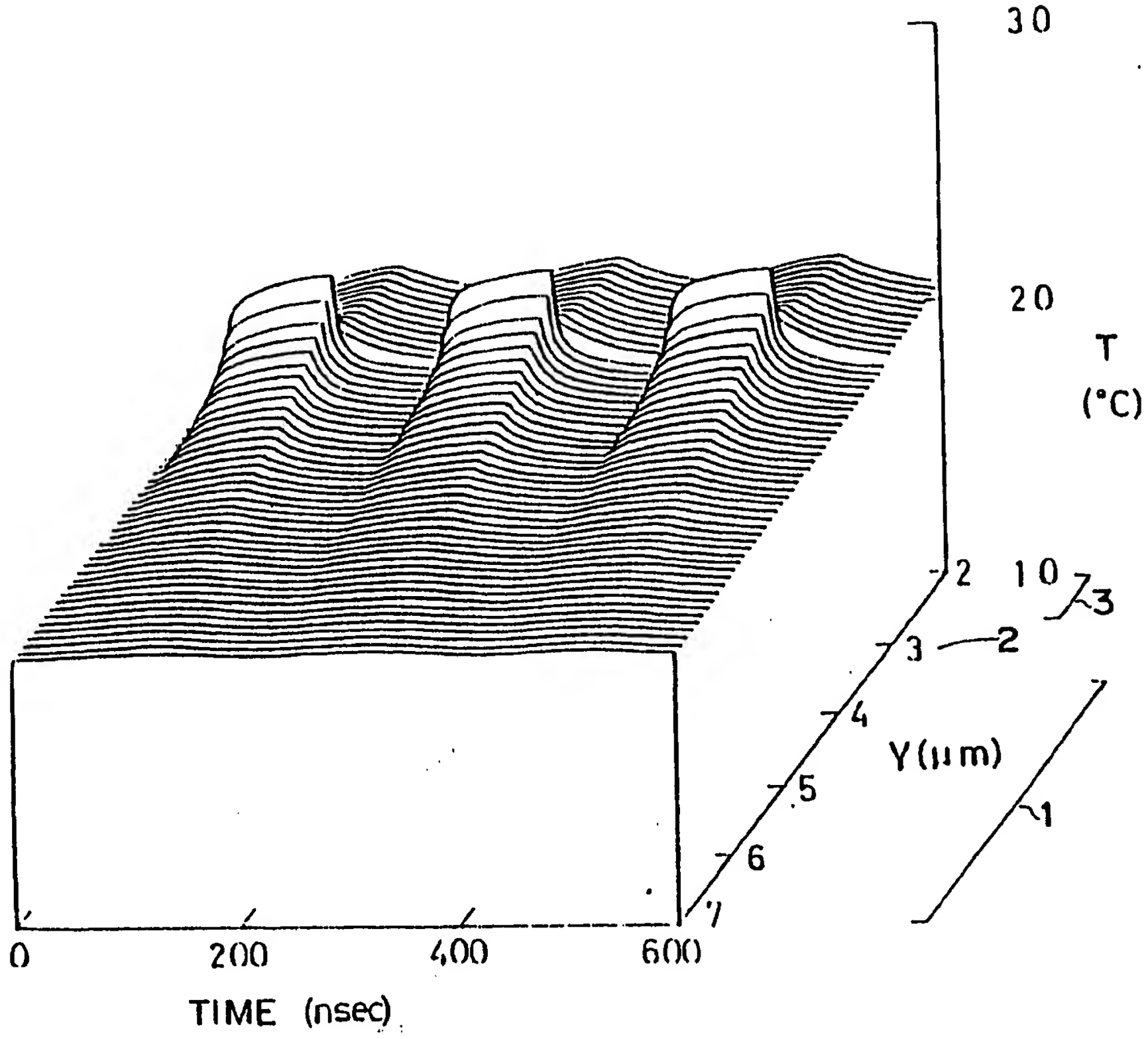


FIG. 8

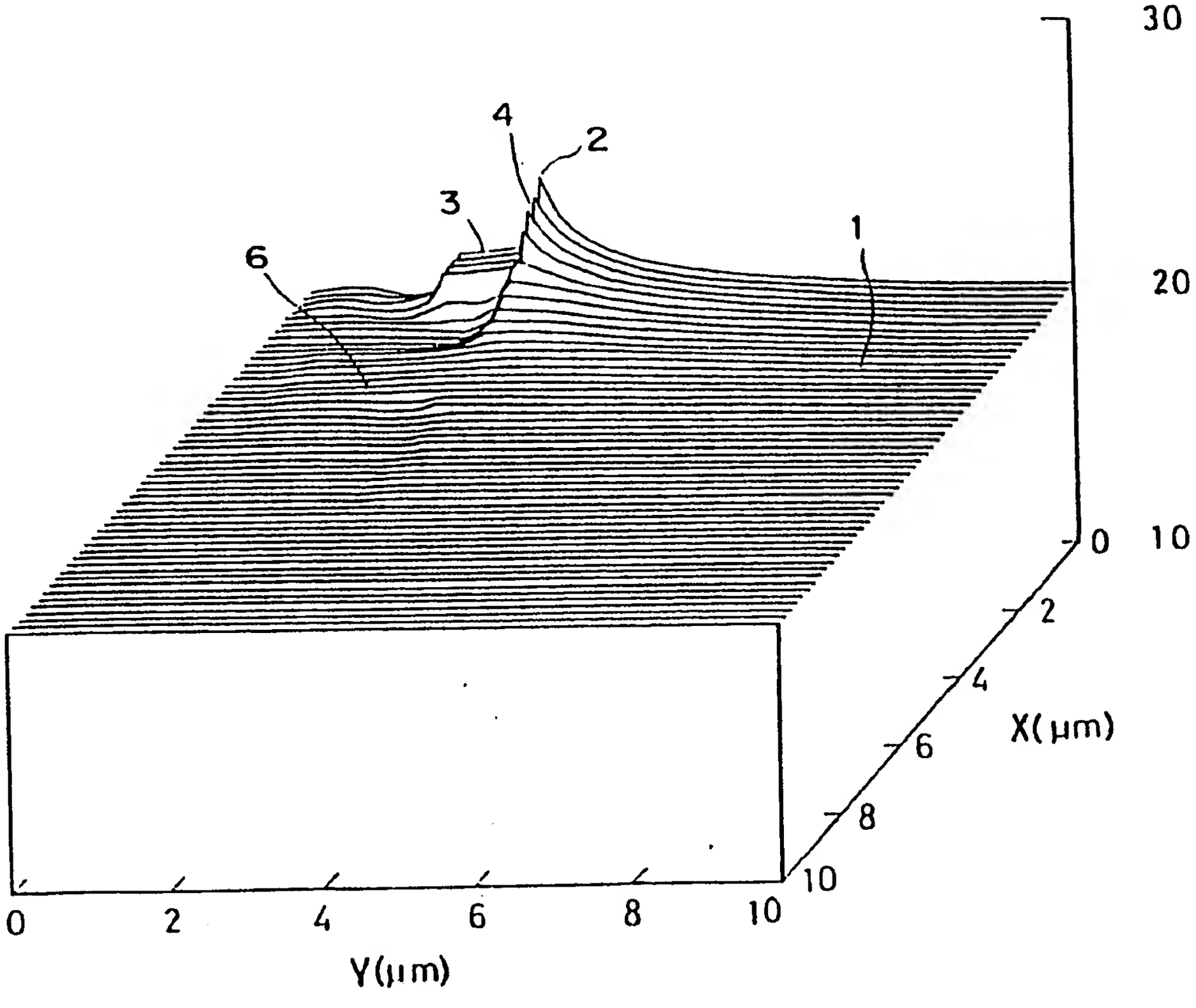


FIG. 9

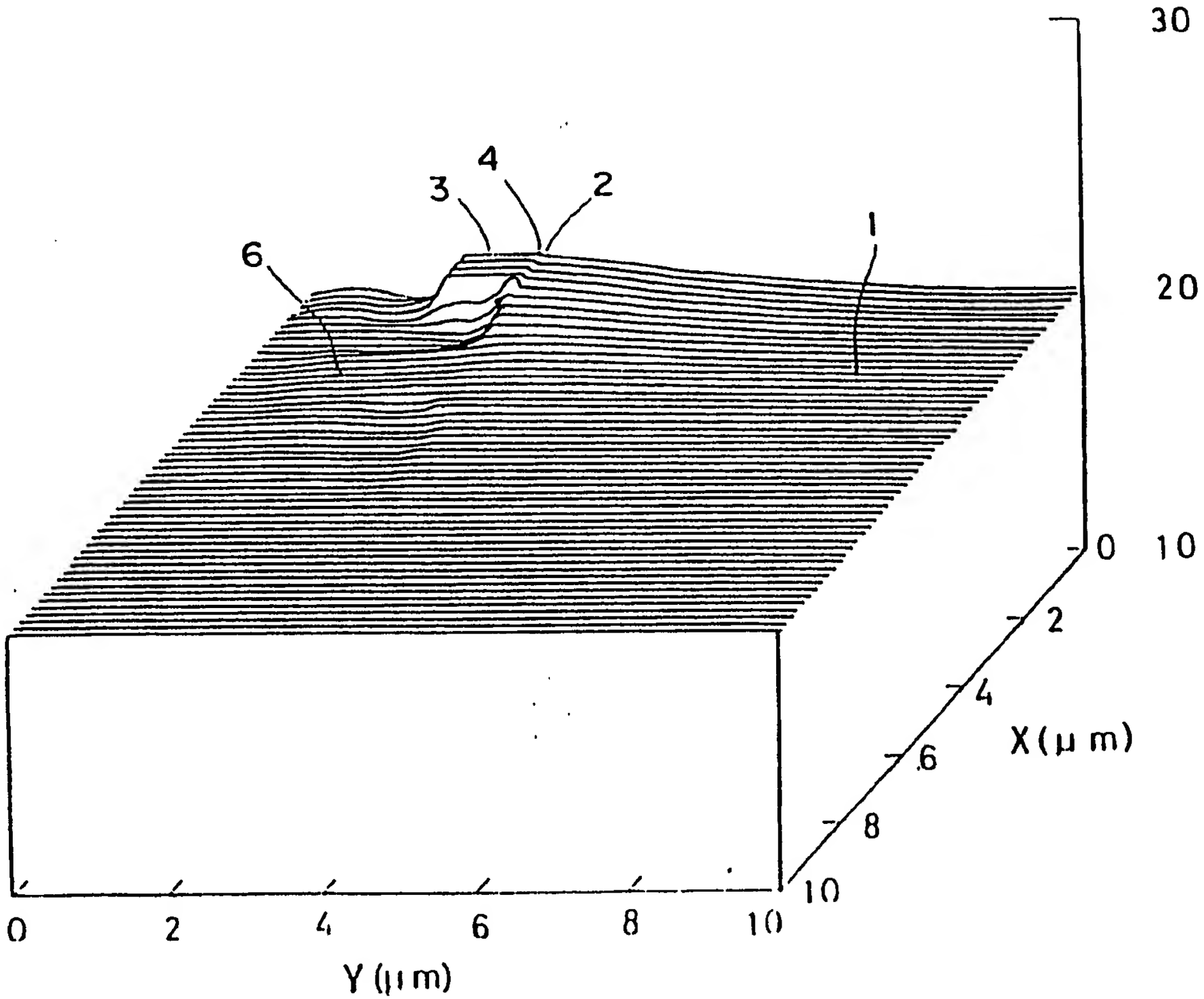


FIG. 10

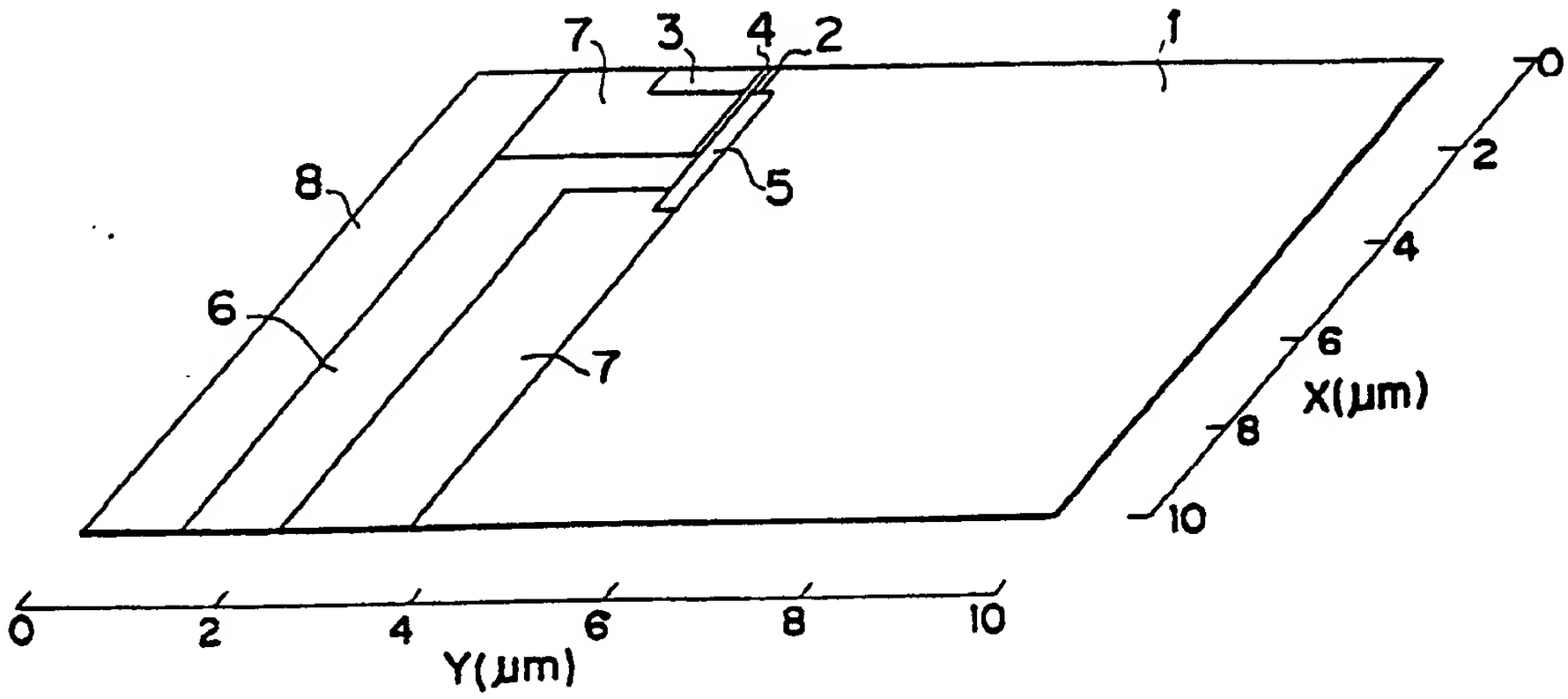


FIG. 11
PRIOR ART

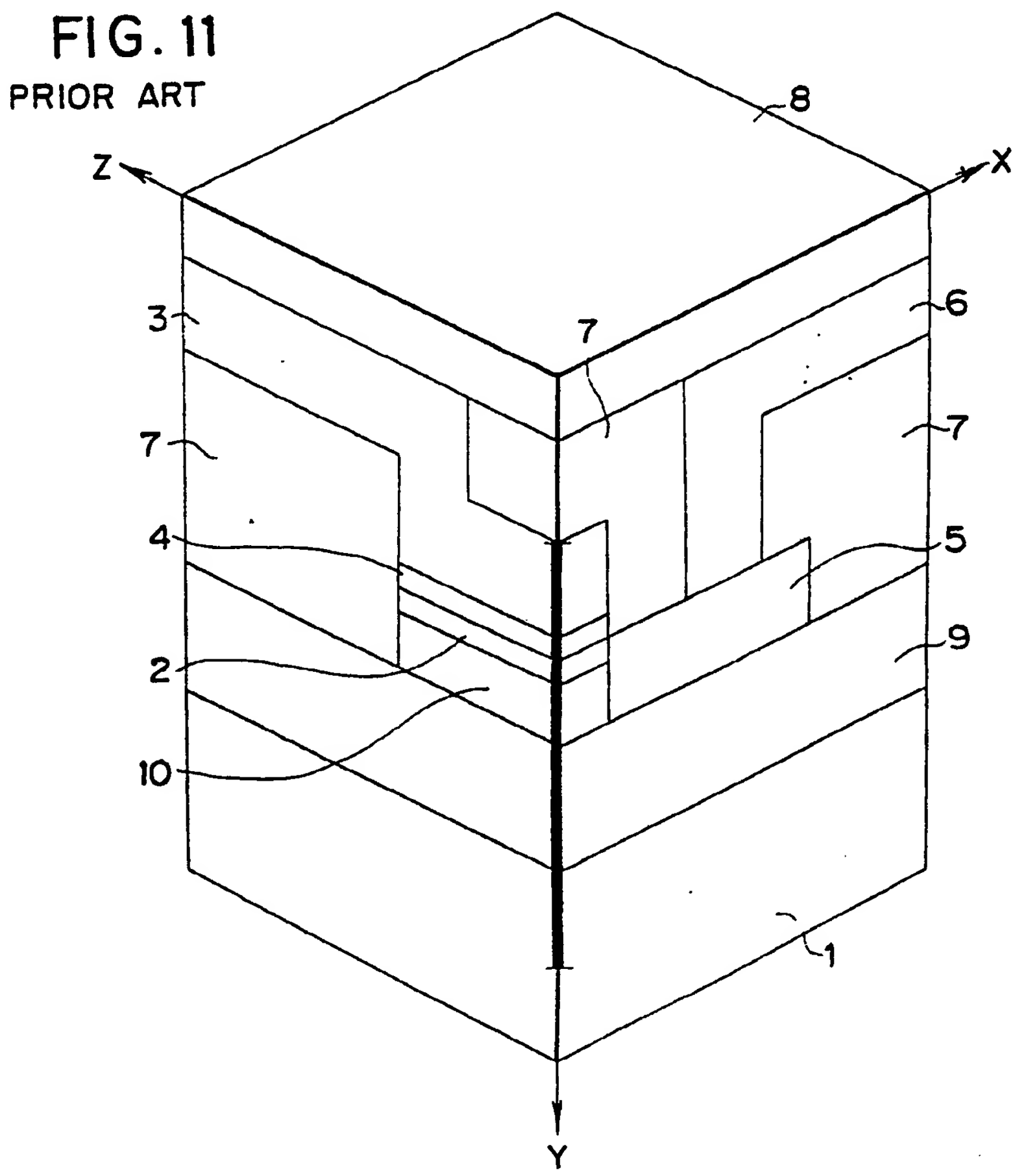


FIG. 12

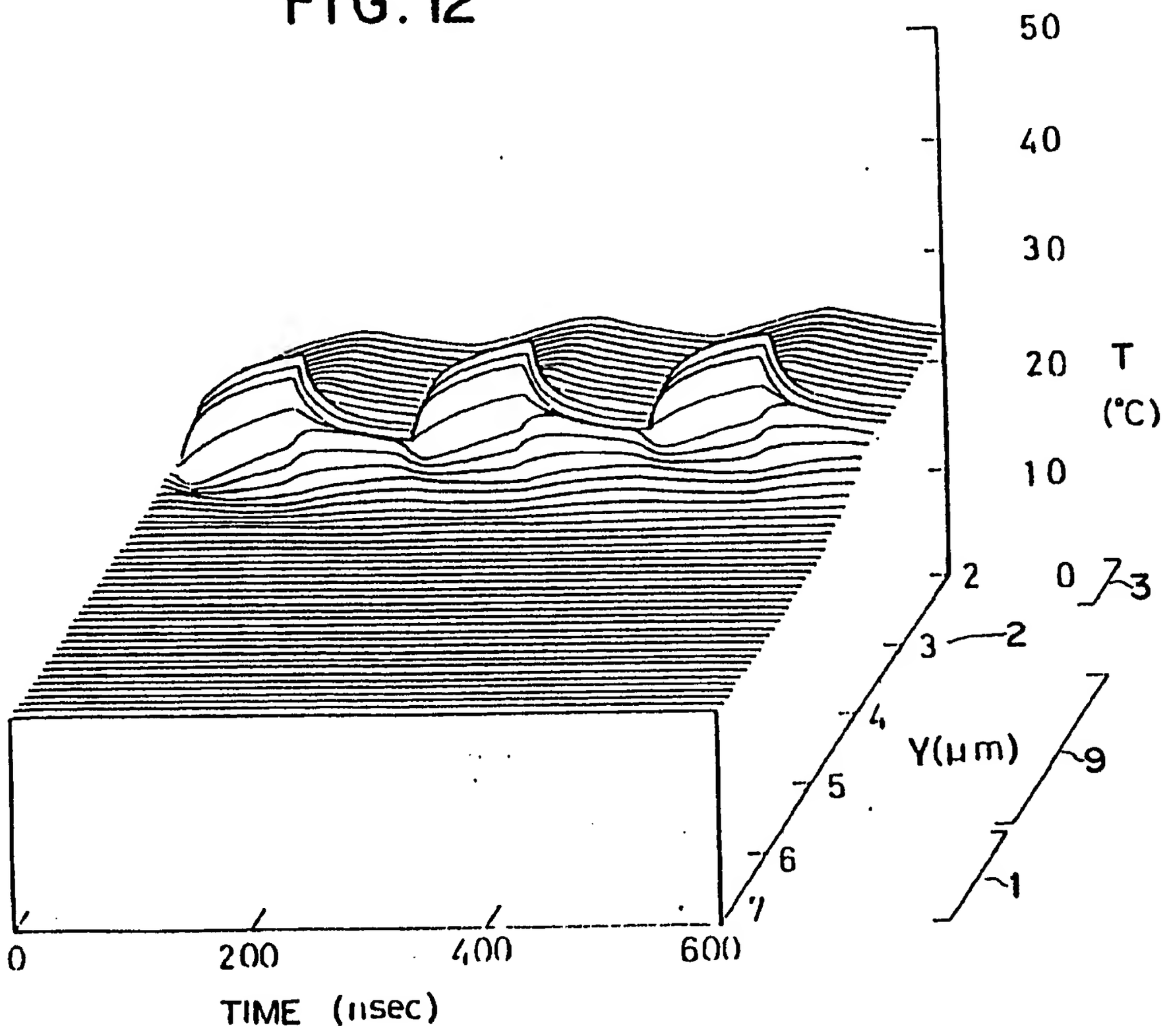


FIG. 13

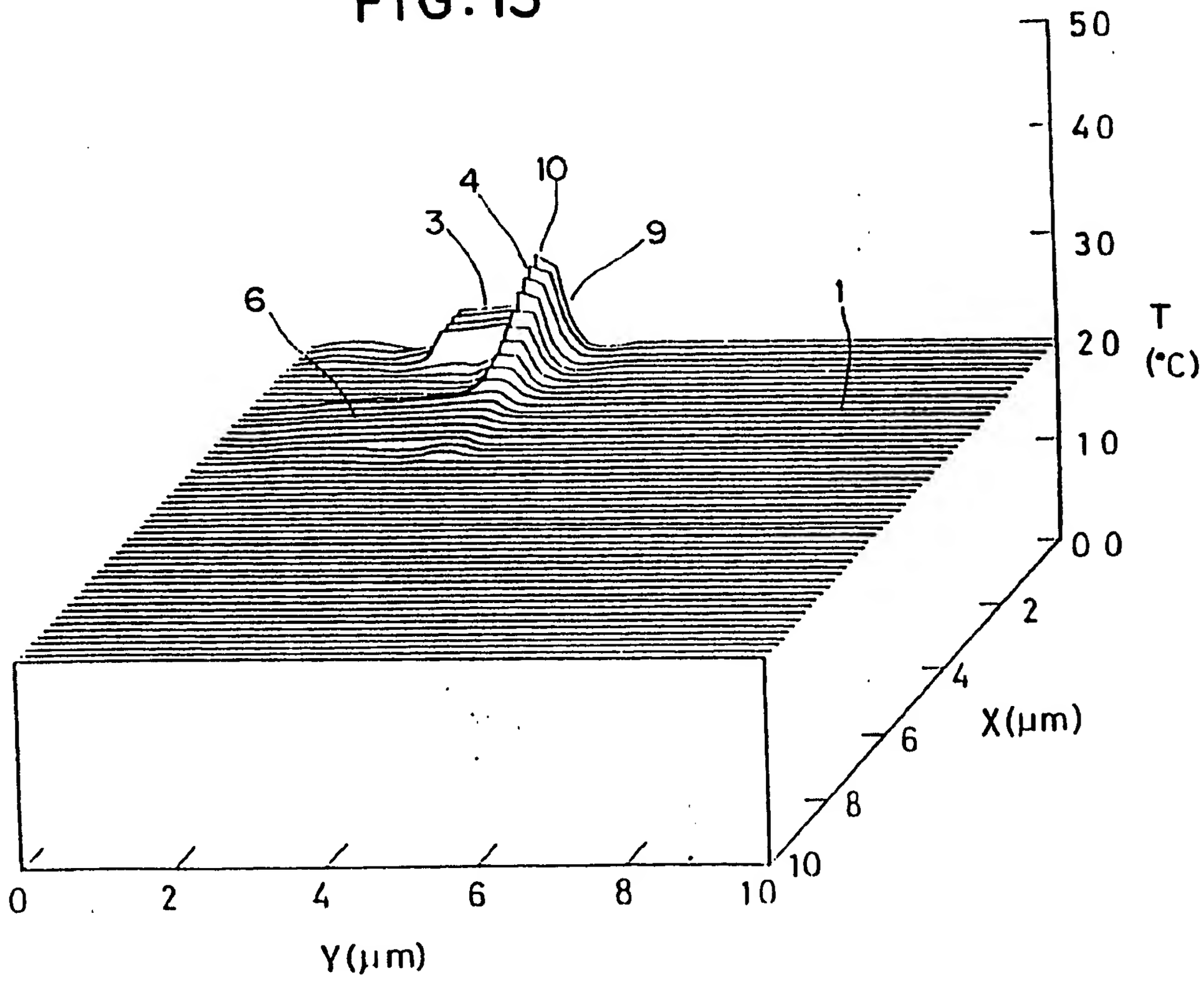


FIG.14

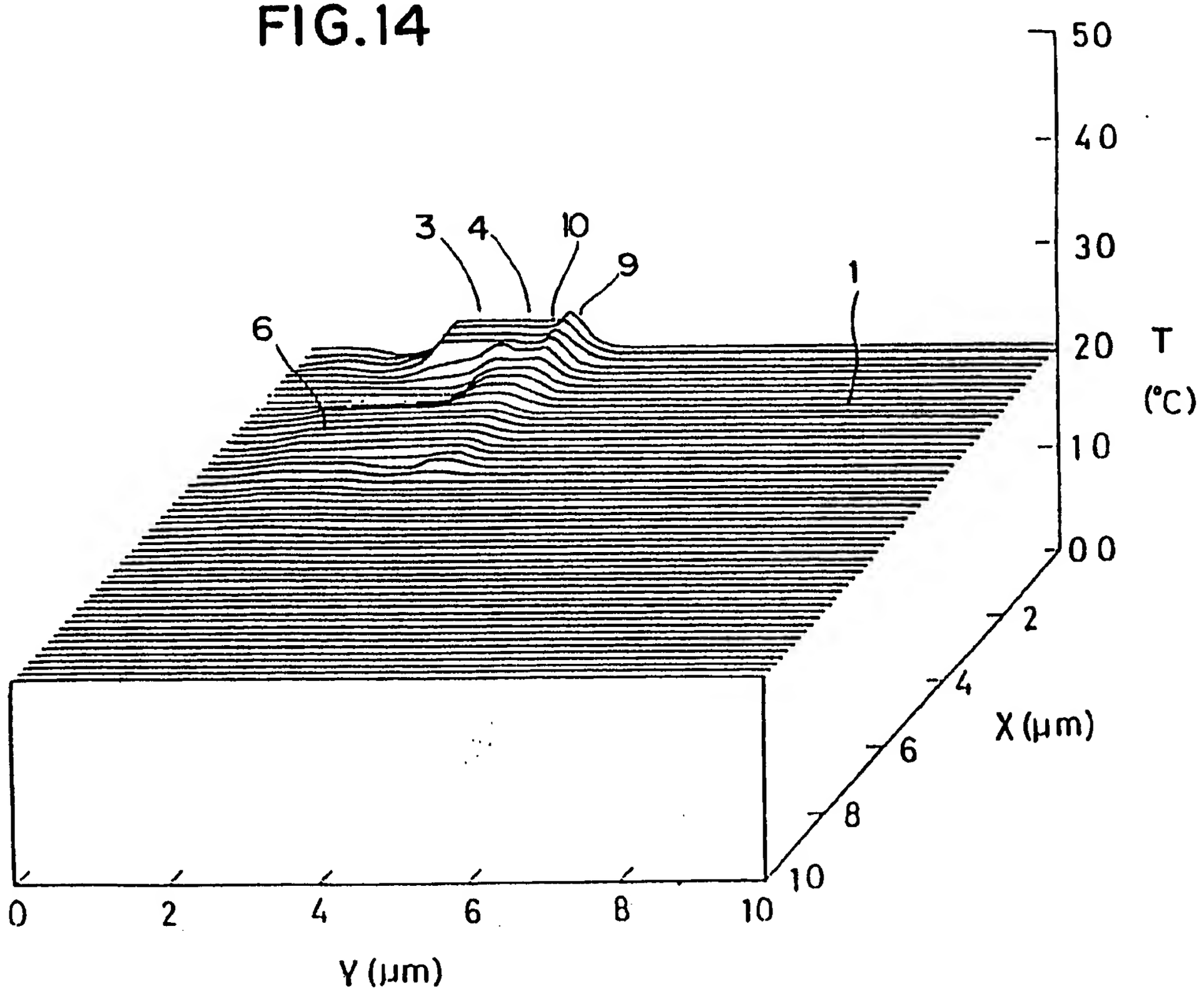
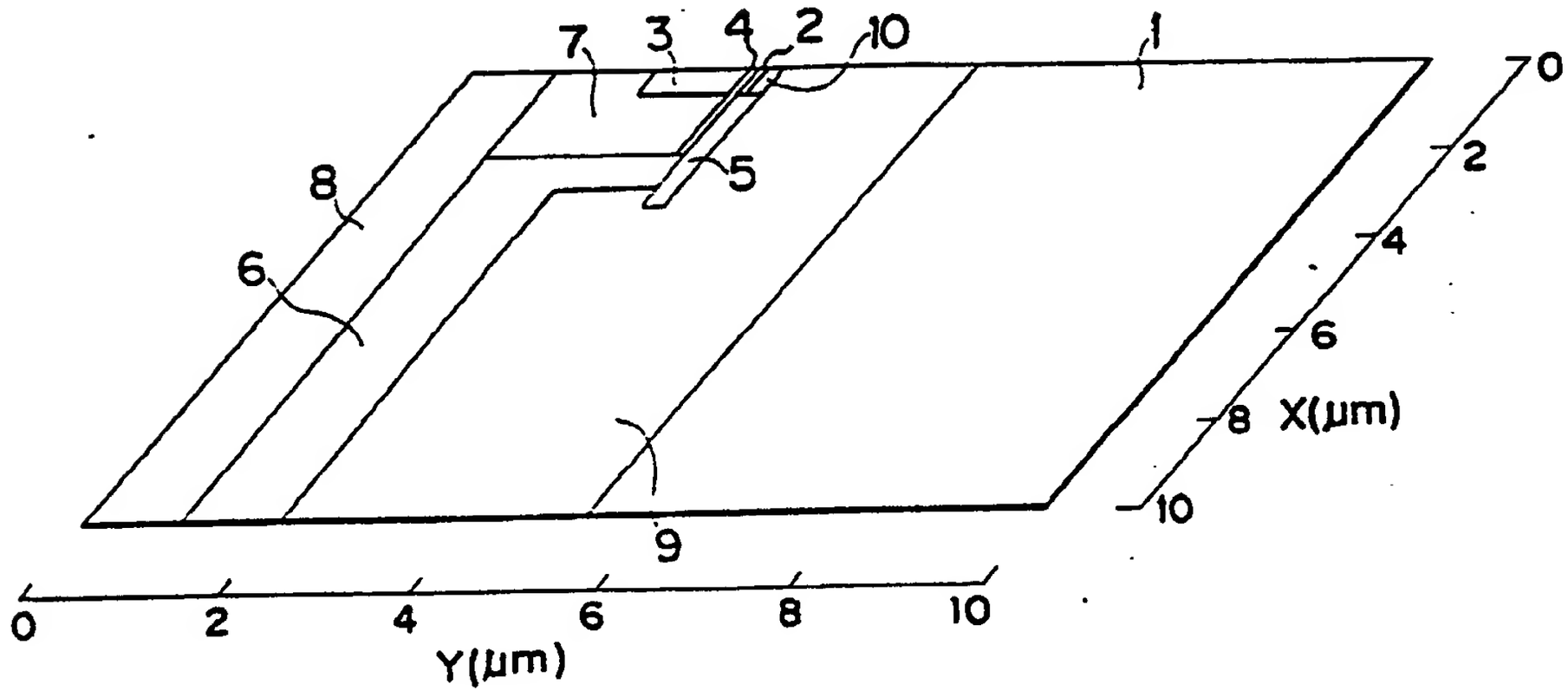


FIG. 15



COOLING SEMICONDUCTOR DEVICES

This invention relates to cooling semiconductor devices, and more particularly to an improvement using an arrangement suitable for heat discharge and cooling of the semiconductor device itself for purposes of establishing an ultra-high speed, ultra-high integrated electronic circuit.

Incorporation of semiconductor integrated circuits into an integrated circuit has been developed to meet requirements of a ultra-high speed and a ultra-high density. However, a limit of heat discharge now prevents a further integration density of integrated circuits which consume large power for high speed operations.

A logic circuit, for example, among presently used semiconductor integrated circuits, has the integration rate of 1500 gates per chip approximately. Its power consumption per gate is about 1mW, and heat of about 1w is generated per chip. This amount of heat is near the limit of heat charge by normal air-cooling, and it is difficult to further develop such integration by merely diminishing the sizes of elements.

In contrast, power consumption per chip is largely increased due to requirements of increasing the efficiency and the speed of a semiconductor integrated circuit. Large part of the consumed power is changed to heat, and the heat increases the temperature of the

entire chip and invites deterioration of the characteristic and the reliability of the element. Since the heating generating portion is a very small operative region and the operation speed is very high, local and transient changes in the temperature are serious problems. Therefore, an existing heat discharging or radiating circuit designed for dealing with static, large regions is not sufficient at all, and the industry desires a high speed heat flow circuit suitable for dynamic, very small regions as well, considering transient conditions of the element during operation.

The problem of heat discharge of an existing semiconductor element is explained below, referring to drawings.

Figures 6 through 10 show existing MOS FET elements using silicon (Si).

The MOS FET element of Figure 6 has a typical structure. Since the structure is symmetrical, Figure 6 shows a quarter of one MOS FET element. Reference numeral 1 denotes a substrate made from p-Si, for example. Numeral 2 refers to a channel, and 3 to a gate electrode made from polycrystalline Si. Numeral 4 denotes a gate insulating layer made from, for example, silicon oxide SiO_2, and numeral 5 designates a source or drain made from, for example, n^+Si. Numeral 6 indicates a wiring made from, for example, Al. Numeral 7 designates an insulating layer made from, for example, SiO_2. Numeral 8 denotes an insulating layer made from, for example, SiO_2. In this typical arrangement, the gate length is 1.3μm, and the gate width is 5μm. The driving

pulse current may be in a standard form of clock frequency 5mHz and pulse width 100n sec (100 nanoseconds).

The thickness of the channel under the gate is about 8nm. The aforementioned pulse current causes generation of Joule heat of heat generating rate 2.9mW near the channel. The initial temperature of the entire element is 20°C, and the surface of the insulating layer 8 discharges heat due to natural convection (heat transfer coefficient $10^{-3}W/cm^2°C$).

Figure 7 shows how the temperature T changes with time around the channel of the MOS FET element. In response to ON and OFF changes of a pulse current, the temperature around the channel exhibits a transient change of n sec. order in a local region of μm order.

Figure 8. shows a temperature distribution of an X-Y plan view of Figure 9 at the time 100n sec. later than application of the pulse current, i.e. just after the pulse current is cut off.

The temperature increase of the channel 2 at this time is about 4°C. However, considering that a significantly large temperature gradient as much as 100°C/μm approximately is produced in the depth direction (Y direction) in the gate insulating layer 4 and that temperature changes are responsive every several nanoseconds, the resulting local transient heat stress is very large.

Figure 9 shows a temperature distribution of the X-Y plan view at the time 110n sec. later than application of the pulse current, i.e. 10n sec. later than the pulse current is cut off.

After the pulse current is cut off, the temperature near the channel suddenly drops. Thus in the conventional arrangement of MOS FET element, locally, transiently large temperature changes occur near the channel, and a new heat flow circuit arrangement is required to remove this.

Figures 11 through 15 conventional SOI (silicon on insulator) arrangements for MOS FET elements.

In the MOS FET element having the SOI arrangement of Figure 11, numeral 9 denotes an insulating layer for the SOI arrangement which may be, for example, a SiO_2 layer of thickness 2μm. Numeral 10 designates a semiconductor active layer for the SOI arrangement which may be a typical p-Si layer of thickness 0.3μm and area 5 x 7μ m^2 as illustrated. The remainder arrangement is similar to the MOS FET element of Figure 6. To the element of Figure 11 is fed a pulse current similar to that in the example of Figures 6 through 10.

Figure 12 shows changes in the temperature with time around the silicon active layer and the channel of the aforegoing element. Also in this case, the temperature around the channel 2 exhibits a locally, transiently violent change in response to ON and OFF changes of the pulse current.

Figure 13 shows a temperature distribution of a portion shown in Figure 15 at the time 100n sec. later than application of the pulse current, i.e. just after the pulse current is cut off. In this SOI-arranged MOS FET element, the temperature around the channel 2 is elevated much higher than the above-indicated MOS FET

element on the Si substrate, because the heat conduction rate of the insulating layer (Si_2) 9 is smaller by two digits or so than Si, heat discharge to the substrate is prevented, and the heat remains in the silicon active layer 10.

The temperature of the channel 2 is about 30°C, 100n sec. later than application of the pulse, and it is higher by 6°C approximately than the MOS FET element on the Si substrate. Further, in the width of the gate insulating layer 9, a temperature gradient of about 170°C/μm is produced in the Y direction, that is, a larger heat stress than the case of the MOS FET element on the Si substrate is generated.

Figure 14 shows a temperature distribution of an X-Y plane portion also shown in Figure 15 at the time 150n sec. later than application of the pulse current, i.e. 50n sec. later than the pulse current is cut off. As compared to Figure 10 , heat remains.

Therefore, in case of the SOI arrangement, heat discharge from the channel 2 to the Si substrate is prevented by the insulating layer 9, and a new heat flow circuit arrangement is required to remove the heat.

It is therefore an object of one embodiment of the invention to provide a semiconductor device having a heat flow circuit capable of removing heat from semiconductor elements.

The present invention provides a semiconductor device comprising a semiconductor chip including a substrate and a plurality of heat emissive semiconductor elements formed on the surface portion of said substrate· said semiconductor chip containing a thermally conductive layer so formed on said chip

as to cover said elements and as to be at least locally in proximity of said elements in order to conduct and spread heat flow produced from said elements by a heat flow circuit having said thermally conductive layer; a first thermally conductive plate provided with said chip; and a heat discharging fin attached to the opposite side of said plate to said chip.

Even if the temperature is increased transiently and locally in a heat generating element, the heat is immediately removed by the heat flow circuit including the layer of good thermal conductivity and good electrical conductivity material.

Examples of the invention will now be described with reference to the drawings, in which:-

Figures 1 is a schematic view of a semiconductor device having heat generating elements;

Figure 2 is a schematic view of a semiconductor device having heat generating elements;

Figure 3 is a schematic view of a semiconductor device having heat generating elements;

Figures 4 and 5 are schematic views of two embodiments of the present invention;

Figure 6 through 10 are views for explaining problems of a conventional MOS FET element;

Figure 11 through 15 are views for explaining problems of a conventional SOI-arranged MOS FET element;

Figure 1 shows a planar type heat flow circuit as a local, transient heat flow circuit throughout the entire chip. In the same drawing, a heat generating element 15 is provided on a substrate 14, and a layer 16 formed of material having a good thermal conductivity and good electrical insulation properties is provided to cover them. The substrate 14 may be of Si, GaAs, InP, Al_2O_3 or any other material suitable for forming the heat generating element 15. In this case, the heat generating

element 15 may be any semiconductor element such as MOS type transistor, bipolar type transistor, semiconductor laser, light emitting diode, etc. which has a property of a local, transient heat generating source.

The layer 16 may be of any material which has a heat conduction ratio equivalent to a metal and which is an insulator. For example, AlN, BN or the like is preferable. Locally, transiently variable heat generated around the heat generating element 15 is averaged by the planar type heat flow circuit including the layer 16, heat stress is removed, and at the same time, a heat discharge circuit or a cooling circuit (both not shown) provided on the layer 16 efficiently discharges heat to the exterior before the heat extends to the entire chip.

The above-indicated method can also be used in a device in which the heat generating element or the semiconductor chip has a three-dimensional multi-layer structure.

Figure 2 shows a metal-wiring-combined heat flow circuit including the same substrate 14 and heat generating element 15 as those in Figure 1. Locally, transiently variable heat generated around the heat generating element 15 is pumped out by a metal wiring 17. Numeral 18 designates an insulating layer made from a material having good thermal conductivity and good electrical insulation properties. Therefore, in this case, heat is pumped up from the heat generating element 15 by the metal wiring 17, it is subsequently averaged by the layer 16, and it is efficiently discharged to the exterior by a heat discharge circuit or a cooling circuit (both not shown) provided on the layer 16.

Figure 3 shows a through-hole type heat flow circuit. On the substrate 14 is provided a semiconductor element 15 which generates heat according to its purposes.

The substrate 14 may be of any material such as Si, GaAs, InP, Al_2O_3, SiO_2 or the like which is suitable for forming the heat generating element 15. In this case, the heat generating element 15 may be any semiconductor element such as MOS type transistor, bipolar type transistor, semiconductor laser, light emitting diode, etc. which has a property of a local, transient heat generating source.

Although the heat flow circuit is readily configured into a planar type in the arrangement of Figure 1, the periphery of the heat generating element normally has undulations due to the presence of a multi-layer wiring of a mesa construction and this prevents direct provision of such a planar thermally conductive layer.

Therefore, a through hole is formed in the insulating layer 18 up to a portion near the heat generating element, and a thermally conductive layer 19 is formed in the hole. The thermally conductive layer 19 may be of a metal unless it degrades the electric characteristic of the heat generating element 15. In most cases, the layer 19 in the form of such a thermally conductive and electrically conductive layer is designed more easily, and maybe configured to directly contact the heat generating element 15. The thermally conductive and electrically insulating layer can be made from AlN, BN, etc. for example.

In the example of Figure 3, a further through hole is provided in the substrate, and a thermally conductive layer 20 is formed therein, so that heat is removed from the substrate side as well. However, the device is effective, with the through hole type heat flow circuit 19 or 20 alone.

The thermally conductive layer 20 may be of a metal unless it degrades the electric characteristic of the heat generating element 15. In most cases, the layer 20 in the form of a thermally conductive and electrically insulating layer is designed more easily, and may be configured to directly contact the heat generating element 15. The thermally conductive and electrically insulating layer can be made of AlN, BN, etc. for example.

A heat discharge circuit or a cooling circuit (both not shown), which is provided next to the layers 19 and 20, efficiently discharges the heat to the exterior before the heat extends to the entire chip.

Figure 4 shows one embodiment of the present invention which uses a heat discharge circuit in the form of an air cooling fin.

A chip 21 includes the aforementioned heat flow circuit, and the heat generating element in the chip is a semiconductor element such as MOS type transistor, bipolar type transistor, semiconductor laser, light emitting diode, etc. which generates heat locally and transiently due to its high speed operation. In order to connect the chip 21 to a heat radiating fin 24, it is designed to remove heat from both the front and back sides of the chip. One side of the chip is attached to a thermally conductive plate 22 (preferably of an electrical insulator such as AlN, BN, etc. in most cases, or an Al or Cu plate, etc. if a metal is employable), and heat is transmitted to the heat radiating fin 22. The other side of the chip is covered by the thermally conductive layer 23 (of AlN, BN, etc. for example) to fill a gap between the thermally conductive plate 26 and itself, and heat is transmitted to a heat radiating fin 27.

Numeral 25 designates a mount board. Since the local, transient heat generated in the chip is discharged to the exterior in this fashion before the heat extends in

the transversal direction of the chip, high speed operation is stabilised.

Figure 5 shows another heat discharge or cooling circuit. As is used in the arrangement of Figure 4, numeral 21 refers to a chip 22 to a thermally conductive plate, 23 to a thermally conductive layer, 24 and 27 to heat radiating fins, and 25 to a mount board. In this embodiment, coolant 28 flows along a coolant circulating tube 29. The coolant 28 may be any material suitable for cooling, such as Freon, water, etc.

Thus this embodiment can efficiently remove from the chip a much more amount of heat than in the air cooling, and ensures a more stable high speed operation.

As described above, where a semiconductor element itself or a semiconductor chip includes a heat flow circuit which is responsive transiently and capable of removing heat from small regions, the integrating density of electronic circuits is increased, high speed operation is stabilised, and functions of the semiconductor element are remarkably enhanced.

CLAIMS

1. A semiconductor device comprising a semiconductor chip including a substrate and a plurality of heat emissive semiconductor elements formed on the surface portion of said substrate; said semiconductor chip containing thermally conductive layer so formed on said chip as to cover said elements and as to be at least locally in proximity of said elements in order to conduct and spread heat flow produced from said elements by a heat flow circuit having said thermally conductive layer; a first thermally conductive plate provided with said chip; and a heat discharging fin attached to the opposite side of said plate to said chip.

2. A semiconductor device according to Claim 1 wherein said chip attached to said thermally conductive plate is covered by said thermally conductive layer.

3. A semiconductor device according to Claim 2 which further includes a second thermally conductive plate so provided as to contact with said thermally conductive layer, and a heat discharging fin attached to the opposite side face of said second thermally conductive plate to the face contacting with the thermally conductive layer.

4. A semiconductor device device as hereinbefore described with reference to either of Figures 4 or 5 of the drawings.

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